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Method for forming isolation layer of semiconductor device

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Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2001108828	A	20011208	KR 200029766	A	20000531	200240	B

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Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001108828	A		1	H01L-021/76	

Abstract (Basic): KR 2001108828 A

NOVELTY - An isolation layer formation method is provided to reduce a parasitic transistor and a leakage current by rounding edge portions of an STI(Shallow Trench Isolation).

DETAILED DESCRIPTION - After sequentially forming and patterning a pad oxide(12) and a pad nitride(13) on a silicon substrate(11), a shallow trench region is defined. The top edges of the shallow trench are opened to 100-200 Angstrom by blanket-etching of the pad nitride(13). The edges of top and bottom portions of the shallow trench are rounded by an RTA(Rapid Thermal Annealing) under hydrogen(H2) gas atmosphere. After forming a liner oxide(14) on the resultant structure, an HDP (High Density Plasma) oxide (15) is filled and densified.

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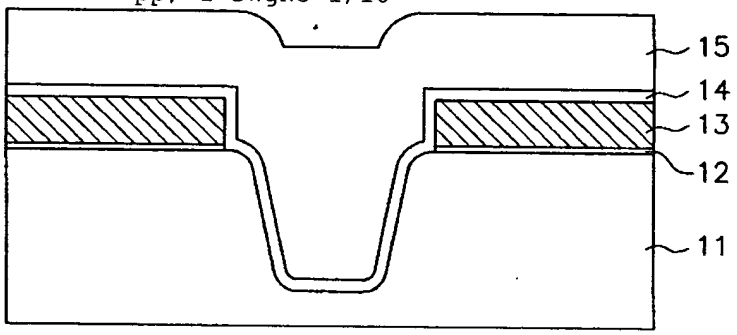

Title Terms: METHOD; FORMING; ISOLATE; LAYER; SEMICONDUCTOR; DEVICE
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